FEE TRANSMITTAL

MAY 06 2008 PATENT & TRADEMARK OFFICE

	Complete if Known	
	Application Number	10/705,347
	Filing Date	11/08/2003
	First Named Inventor	Labelle
	Examiner Name	CHEN, Kin Chan
☐ Applicant claims small entity status. See 37 CFR 1.27	Art Unit	1792
TOTAL AMOUNT OF PAYMENT $630.00	Attorney Docket No.	0180151

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account · Deposit Account Number: **50-0731** Deposit Account Name: **Farjami & Farjami LLP**

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims		Fee ($)		Fee Paid ($)
	- 20 or HP =	0	x	$50.00	=	$ 0.00

HP = highest number of total claims paid for, if greater than 20

Indep. Claims		Extra Claims		Fee ($)		Fee Paid ($)
	- 3 or HP =	0	x	$200.00	=	$ 0.00

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims Fee ($)	Fee Paid ($)
$360.00	

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41 (a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof		Fee ($)		Fee Paid ($)
	- 100 =	0	/ 50 =	0	(round up to a whole number) x	$250.00	=	$ 0.00

4. OTHER FEE(S) Fees Paid($)

Non-English Specification, $130 fee (no small entity discount)

Other: **Filing a brief in support of an appeal and one (1) month extension fee** **$630.00**

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 38,135	Telephone (949) 282-1000
Name (Print/Type)	Michael Farjami, Esq.		Date 4/30/08

05/06/2008 NNGUYEN1 00000081 10705347

02 FC:1251 120.00 OP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Labelle, et al.**	Art Unit: 1792
Serial No.: 10/705,347	Examiner: Chen, Kin Chan
Filed: November 8, 2003	
For: **Method for Integrating a High-K Gate Dielectric in a Transistor Fabrication Process**	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is an Appeal from the Examiner's Final Rejection of claims 21-34. The Final Rejection issued on November 19, 2007. The Notice of Appeal was filed in the U.S. Patent and Trademark Office on February 13, 2008.

REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc.

RELATED APPEALS AND INTERFERENCES

Appeal No. 2007-0287 in above-referenced patent application was decided on March 16, 2007. A true and correct copy of this Decision on Appeal dated March 16, 2007 is enclosed as the "Related Proceedings Appendix," and filed herewith.

STATUS OF CLAIMS

Claims 21-34 are pending, and claims 1-20 were canceled in previous amendments. Claims 21-34 have been finally rejected in a Final Rejection dated November 19, 2007. This Appeal is directed to the rejection of claims 21-34. Claims 21-34 appear in an Appendix to this Appeal Brief.

STATUS OF AMENDMENTS

No claim amendments have been entered after issuance of the Final Rejection of November 19, 2007.

SUMMARY OF CLAIMED SUBJECT MATTER

A. Claim 21

Independent claim 21 defines a method for forming a field-effect transistor on a substrate (e.g., substrate 104 in Figure 1) including forming a high-k dielectric layer (not shown in Figure 1) over the substrate and a gate electrode layer (not shown in Figure 1) over the high-k dielectric layer. *See*, e.g., page 7, lines 14-16 and Figure 1of the present application.

The method further includes etching (e.g., step 202 of flowchart 200 in Figure 2) the gate electrode layer and the high-k dielectric layer in a plasma process chamber to form a gate stack (e.g., gate stack 102 in Figure 1). *See*, e.g., page 7, lines 12-14 and 16-18 and Figures 1 and 2 of the present application. The gate stack (e.g., gate stack 102 in Figure 1) includes a high-k dielectric segment (e.g., high-k dielectric segment 106 in Figure 1) situated over the substrate (e.g., substrate 104 in Figure 1) and a gate electrode segment (e.g., gate electrode segment 108 in Figure 1) situated over the high-k dielectric segment (e.g., high-k dielectric segment 106 in Figure 1).

The method further includes performing a nitridation process (e.g., step 204 of flowchart 200 in Figure 2) in the process chamber immediately after the step of etching the gate electrode layer and the high-k dielectric layer, where the nitridation process utilizes a nitrogen containing plasma to nitridate sidewalls (e.g., sidewalls 110 in Figure

1) of the high-k dielectric segment (e.g., high-k dielectric segment 106 in Figure 1). *See*, e.g., page 7, lines 20-22, page 8, lines 9-10, and Figure 1 of the present application. The nitridation process on the high-k dielectric segment causes nitrogen to ender the high-k dielectric segment, where the nitrogen forms an oxygen diffusion barrier in the high-k dielectric segment and prevents lateral diffusion of oxygen into the high-k dielectric segment. *See*, e.g., page 8, lines 14-18 and Figure 1 of the present application.

The method further includes repairing damage on the sidewalls (e.g., sidewalls 110 in Figure 1) of the high-k dielectric segment (e.g., high-k dielectric segment 106 in Figure 1) caused during the step of etching the gate electrode layer and the high-k dielectric layer. *See*, e.g., page 8, lines 11-14 and Figure 1 of the present application.

B. Claim 28

Independent claim 28 defines a method for forming a field-effect transistor including a high-k dielectric layer (not shown in Figure 1) situated over a substrate (e.g., substrate 104 in Figure 1) and a gate electrode layer (not shown in Figure 1) situated over the high-k dielectric layer. *See*, e.g., page 7, lines 14-16 and Figure 1of the present application.

The method further includes etching (e.g., step 202 of flowchart 200 in Figure 2) the gate electrode layer (not shown in Figure 1) and the high-k dielectric layer (not shown in Figure 1) to form a gate stack (e.g., gate stack 102 in Figure 1). *See*, e.g., page 7, lines 12-14 and 16-18 and Figure 1 of the present application. The gate stack (e.g., gate stack

102 in Figure 1) includes a high-k dielectric segment (e.g., high-k dielectric segment 106 in Figure 1) situated over the substrate (e.g., substrate 104 in Figure 1), a gate electrode segment (e.g., gate electrode segment 108 in Figure 1) situated over the high-k dielectric segment (e.g., high-k dielectric segment 106 in Figure 1), and includes sidewalls (e.g., sidewalls 110 in Figure 1).

The method further includes utilizing a nitrogen plasma is utilized to nitridate (e.g., step 204 of flowchart 200 in Figure 2) the sidewalls (e.g., sidewalls 110 in Figure 1) of the gate stack (e.g., gate stack 102 in Figure 1) immediately after the step of etching the gate electrode layer and the high-k dielectric layer. *See*, e.g., page 7, lines 19-22, page 8, lines 9-10, and Figure 1 of the present application. The step of etching the gate electrode layer and the high-k dielectric layer to form the gate stack is performed in a process chamber being utilized to perform the step of performing the nitridation process on the gate stack. *See*, e.g., page 7, line 22 through page 8, line 2 of the present application.

The method further includes repairing damage on the sidewalls of the gate stack caused during the step of etching the gate electrode layer and the high-k dielectric layer. *See*, e.g., page 8, lines 11-14 and Figure 1 of the present application. The method further includes forming source/drain regions adjacent to the gate stack (e.g., gate stack 102 in Figure 1), fabricating spacers on the sidewalls (e.g., sidewalls 110 in Figure 1) of the gate stack, and performing a rapid thermal anneal on the gate stack. See, e.g., page 9, lines 2-4 of the present application.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 21-34 under 35 USC §103(a) as being unpatentable over U.S. Patent Application Publication No. 2005/0079696 to Luigi Colombo (hereinafter "Colombo") in view of U.S. Patent No. 6,265,260 to Alers et al. (hereinafter "Alers"), or U.S. Patent No. 6,566, 250 to Tu et al. (hereinafter "Tu") as evidenced by U.S. Patent Application Publication No. 2004/0188240 to Chang et al. (hereinafter "Chang '240"), or U.S. Patent No. 6,090,210 to Ballance et al. (hereinafter "Ballance"), or U.S. Patent No. 6,759,337 to Aronowitz et al. (hereinafter "Aronowitz"), or U.S. Patent Application Publication No. 2005/0019964 to Chang et al. (herein after "Chang '964").

ARGUMENT

The Examiner has rejected claims 21-34 under 35 USC §103(a) as being unpatentable over Colombo in view of Alers, or Tu as evidenced by Chang '240, or Ballance, or Aronowitz, or Chang '964.

Appellants respectfully submit that the present invention, as defined by independent claims 21 and 28, is patentably distinguishable over the cited references, either singly or in combination.

By reference to Figures 1 and 2 of the present application, gate stack 102 can be formed in a process chamber by utilizing a plasma etch. In an embodiment of the invention, a nitridation process can be performed by utilizing a nitrogen plasma to

nitridate exposed sidewall surfaces of high-k dielectric segment 106 in gate stack 102 immediately after the gate etch process has been performed in the same process chamber. *See*, e.g., page 7, line 22 and page 8, lines 1-2 and 9-10 of the present application. The nitridation process can be utilized to repair damage to gate stack 102 during the etch process and to form a barrier in high-k dielectric segment 106 to prevent oxygen from laterally diffusing into the high-k dielectric segment during subsequent processing steps.

By performing a nitridation process immediately after the gate etch process, as specified in the independent claims, a barrier in high-k dielectric segment 106 is formed immediately after the gate etch process to promptly prevent oxygen from laterally diffusing into the high-k dielectric segment during subsequent processing steps as well as to repair any gate stack damage to the gate stack resulting from the gate etch process. Also, by performing the gate stack etch and the nitridation processes in the same process chamber, as specified in independent claims 21 and 28, the need to break vacuum is avoided, thereby advantageously providing increased throughput and reduces manufacturing cost.

Colombo specifically discloses a sequence of steps including performing etch process 330 to form a patterned gate structure with top and sidewall surfaces exposed, removing gate mask 328, forming implant mask 333, performing shallow drain extension dopant implant 334, optionally employing a cleaning operation to expose a sidewall portion of gate dielectric 316, and performing nitridation process 335 to nitridate the sidewalls and top of the gate structure. *See*, e.g., pate 4, paragraphs [0028] and [0029]

and Figures 5D through 5F of Colombo. However, Colombo fails to disclose performing a nitridation process immediately after etching a gate electrode layer and a high-k dielectric layer, using a nitrogen containing plasma to nitridate sidewalls of the high-k dielectric segment, and etching the gate electrode and the high-k dielectric layer and performing the nitridation process in the same plasma process chamber, as specified in independent claims 21 and 28.

On pages 3 and 4 of the Final Rejection of November 19, 2007, the Examiner states that since Colombo discloses that the process steps in exemplary method in Fig. 4 may occur in different orders, "... it would have been obvious to one with ordinary skill in the art that the nitridation process may be performed immediately after the step of etching the gate electrode layer and the high-k dielectric layer as claimed in absence of unexpected result or criticality." However, as disclosed in the present application, after the gate etch, the properties of the high-k dielectric material and the transistor gate can be altered by lateral diffusion of oxygen into the high-k gate dielectric during subsequent process steps.

Thus, by performing the nitridation process immediately after the step of etching the gate electrode layer and the high-k dielectric layer, the opportunity for undesirable lateral diffusion of oxygen into the high-k dielectric material and the transistor gate is advantageous limited by the invention as specified in independent claims 21 and 28. In contrast, by disclosing that the process steps in the method in Figure 4 may occur in different orders, Colombo teaches away from any specific advantage that may be

achieved by performing the nitridation process immediately after the step of etching the gate electrode layer and the high-k dielectric layer.

The Examiner relies on Alers and Tu to show a conventional nitridation method of applying plasma comprising nitrogen. On page 3 of the Final Rejection of November 19, 2007, the Examiner states that "[b]ecause it is a conventional method in the art of semiconductor device fabrication and because it is disclosed by Alers, Tu, hence, it would have been obvious to one with ordinary skill in the art to apply said nitridation method in the process of Colombo in order to efficiently carry out the nitridation process." However, the subject matter of Colombo, which is directed to encapsulation and conditioning structures and techniques for MOS transistor gates, is significantly different than the subject matter of Alers and Tu. For example, Alers discloses a method for making an integrated circuit capacitor having a relatively high capacitance including forming a first metal electrode comprising a metal nitride surface and a tantalum pentoxide layer on the metal nitride surface while maintaining a temperature below an oxidizing temperature of the metal, and remote plasma annealing the tantalum pentoxide layer. *See*, e.g., column 1, line 62 through column 2, line 54 of Alers.

Tu, on the other hand, is directed to forming a self-aligned capping layer over a metal filled feature in a semiconductor device by blanket deposition of a first barrier layer over an anisotropically etched feature to prevent diffusion of metal into the substrate; filling the anisotropically etched feature with a metal to form a metal filled feature; planarizing the substrate surface to form an exposed surface of the metal filled feature;

and depositing a second barrier layer to cover the exposed surface of the metal filled feature to form a capping layer. *See*, e.g., column 3, lines 37-53 of Tu. Thus, neither Alers nor Tu remotely suggests application of its disclosure to plasma nitridation of gate stacks in transistors after the gate etch. Thus, Appellants respectfully submit that a person of ordinary skill in the art would not have a sufficient reason to combine Alers and/or Tu with Colombo, as suggested by the Examiner.

On page 4 of the Final Rejection of November 19, 2007, the Examiner acknowledges that Colombo does not specify performing nitridation and etching in the same process chamber and cites Chang '240, Balance, Aronowitz, and Chang '964 as evidence that "... [i]t is common in the art that the plasma process chamber may be used for performing both etching and nitridation because it is efficient and more cost effective." However, the transistor gate disclosed in Colombo is significantly different than the structures disclosed in Chang '240, Balance, Aronowitz, and Chang.

In particular, Chang '240 discloses utilizing a plasma generator for in-situ nitridation and formation of metal salicides. *See*, e.g., the Abstract of Chang '240. Balance discloses a "showerhead" for introducing gas from one or more external supplies into a substrate processing chamber. *See*, e.g., the Abstract of Balance. Aronowitz discloses a process for etching a controllable thickness of oxide formed over a semiconductor substrate by exposing the oxide to a nitrogen plasma in an etch chamber while applying an RF bias to a substrate support on which the substrate is supported in the etch chamber. *See*, e.g., the Abstract of Aronowitz. Chang '964 discloses a method for

determining a composition of an integrated circuit feature on a substrate, including collecting intensity data representative of spectral wavelengths of radiant energy generated by a plasma during plasma nitridation of the integrated circuit feature on the substrate. *See*, e.g., the Abstract of Chang '964.

However, neither Chang '240, Balance, Aronowitz, nor Chang '964 disclose or suggest utilizing a plasma to nitridate a transistor gate stack after a gate etch. Also, since the structures disclosed in Chang '240, Balance, Aronowitz, and Chang '968 are significantly different than the transistor gate disclosed in Colombo, Appellants respectfully submit that, at the time the invention, as defined by independent claims 21 and 28 was made, a person of ordinary skill in the art would not have a sufficient reason or be sufficiently motivated to combine Chang '240, Balance, Aronowitz, and/or Chang '968 with Colombo as suggested by the Examiner.

For the foregoing reasons, Appellants respectfully submit that, at the time the invention defined by independent claims 21 and 28 was made, the invention would not have been obvious to a person of ordinary skill in the art by the references cited by primary reference Colombo, Alers, or Tu singly, or in any of their respective combinations with secondary references Chang '240, Balance, Aronowitz, or Chang '964. the Examiner, either singly or in any combination. Thus, independent claims 21 and 28 are patentably distinguishable over Colombo, Alers, Tu, Chang '240, Balance, Aronowitz, and Chang '964, either singly or in any combination thereof. As such, claims 22-27 depending from independent claim 21 and claims 29-34 depending from

independent claim 28 are, *a fortiori*, also patentably distinguishable over cited references for at least the reasons presented above and also for additional limitations contained in each dependent claim.

CONCLUSION

Based on the foregoing reasons, the present invention as defined by independent claims 21 and 28 and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 21-34 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 21-34 pending in the present application is respectfully requested.

This Appeal Brief is submitted herewith with an Appendix of the appealed claims and the requisite fee for filing the Appeal Brief.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 4/30/08

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Date of Deposit: 4/30/08

Christina Carter Ellis
Name of Person Mailing Paper and/or Fee

Christina Carter Ellis 4/30/08
Signature Date

APPENDIX OF CLAIMS ON APPEAL

Claim 21: A method for forming a field-effect transistor on a substrate, said method comprising:

forming a high-k dielectric layer over said substrate;

forming a gate electrode layer over said high-k dielectric layer;

etching said gate electrode layer and said high-k dielectric layer to form a gate stack comprising a high-k dielectric segment situated over said substrate and a gate electrode segment situated over said high-k dielectric segment, said step of etching said gate electrode layer and said high-k dielectric layer being performed in a plasma process chamber;

performing a nitridation process in said plasma process chamber on said gate stack immediately after said step of etching said gate electrode layer and said high-k dielectric layer, said nitridation process utilizing a nitrogen containing plasma to nitridate sidewalls of said high-k dielectric segment, said nitridation process on said high-k dielectric segment causing nitrogen to enter said high-k dielectric segment, said nitrogen forming an oxygen diffusion barrier in said high-k dielectric segment and preventing lateral diffusion of oxygen into said high-k dielectric segment;

repairing damage on said sidewalls of said high-k dielectric segment caused during said step of etching said gate electrode layer and said high-k dielectric layer.

Claim 22: The method of claim 21 wherein said high-k dielectric layer comprises hafnium oxide.

Claim 23: The method of claim 21 wherein said high-k dielectric layer comprises hafnium silicate.

Claim 24: The method of claim 21 wherein said high-k dielectric layer comprises zirconium oxide.

Claim 25: The method of claim 21 wherein said high-k dielectric layer comprises zirconium silicate.

Claim 26: The method of claim 21 wherein said high-k dielectric layer comprises aluminum oxide.

Claim 27: The method of claim 21 wherein said gate electrode segment comprises polysilicon.

Claim 28: A method for forming a field-effect transistor including a high-k dielectric layer situated over a substrate and a gate electrode layer situated over said high-k dielectric layer, said method comprising steps of:

etching said gate electrode layer and said high-k dielectric layer to form a gate stack, said gate stack comprising a high-k dielectric segment situated over said substrate and a gate electrode segment situated over said high-k dielectric segment, said gate stack comprising sidewalls;

utilizing a nitrogen plasma to nitridate said sidewalls of said gate stack immediately after said step of etching said gate electrode layer and said high-k dielectric layer;

wherein said step of etching said gate electrode layer and said high-k dielectric layer to form said gate stack is performed in a plasma process chamber being utilized to perform said step of performing said nitridation process on said gate stack;

repairing damage on said sidewalls of said gate stack caused during said step of etching said gate electrode layer and said high-k dielectric layer;

forming source/drain regions adjacent to said gate stack;

fabricating spacers on said sidewalls of said gate stack;

performing a rapid thermal anneal on said gate stack.

Claim 29: The method of claim 28 wherein said high-k dielectric layer comprises hafnium oxide.

Claim 30: The method of claim 28 wherein said high-k dielectric layer comprises hafnium silicate.

Claim 31: The method of claim 28 wherein said high-k dielectric layer comprises zirconium oxide.

Claim 32: The method of claim 28 wherein said high-k dielectric layer comprises zirconium silicate.

Claim 33: The method of claim 28 wherein said high-k dielectric layer comprises aluminum oxide.

Claim 34: The method of claim 28 wherein said gate electrode segment comprises polysilicon.

EVIDENCE APPENDIX

(NONE)

RELATED PROCEEDINGS APPENDIX

Enclosed is a true and correct copy of Decision on Appeal No. 2007-0287, dated March 16, 2007 in the above-referenced application.

AMD = H1874 "A"

1180151

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CATHERINE B. LABELLE, BOON-YONG ANG, JOONG S. JEON, ALLISON K. HOLBROOK, QI XIANG, and HUICAI ZHONG

DOCKETED
MAR 19 2007

File RCE
1st. mth. – 4/16/07
2nd. " – 5/16/07

Appeal 2007-0287
Application 10/705,347
Technology Center 1700

Decided: March 16, 2007

Before BRADLEY R. GARRIS, THOMAS A. WALTZ, and CATHERINE Q. TIMM, *Administrative Patent Judges*.

WALTZ, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on an appeal from the Primary Examiner's final rejection of claims 1, 6 through 8, 14 through 16, 19, and 20, which are the only claims pending in this application. We have jurisdiction pursuant to 35 U.S.C. §§ 6 and 134.

According to Appellants, the invention is directed to a method for forming a field-effect transistor on a substrate, where the substrate includes a high-k dielectric layer situated over the substrate, and a gate electrode layer situated over the high-k dielectric layer (Br. 3). The method includes the step of etching the gate electrode layer and the high-k dielectric layer in a plasma process chamber to form a gate stack, followed by a nitridation process using a nitrogen containing plasma in the plasma process chamber to nitridate the sidewalls and form an oxygen diffusion barrier (*id.*). Independent claim 1 is illustrative of the invention and is reproduced below:

1. A method for forming a field-effect transistor on a substrate, said substrate including a high-k dielectric layer situated over said substrate and a gate electrode layer situated over said high-k dielectric layer, said method comprising steps of:

etching said gate electrode layer and said high-k dielectric layer to form a gate stack, said gate stack comprising a high-k dielectric segment situated over said substrate and a gate electrode segment situated over said high-k dielectric segment;

performing a nitridation process on said gate stack, said nitridation process utilizing a nitrogen containing plasma to nitridate sidewalls of said gate stack, said nitridation process on said gate stack causing nitrogen to enter said high-k dielectric segment, said nitrogen forming an oxygen diffusion barrier in said high-k dielectric segment;

wherein said step of etching said gate electrode layer and said high-k dielectric layer to form said gate stack is performed in a plasma process chamber, said plasma process chamber being utilized to perform said step of performing said nitridation process on said gate stack.

The Examiner relies on the following references as evidence of obviousness:

Doyle	US 5,891,798	Apr. 06, 1999
Ballance	US 6,090,210	Jul. 18, 2000
Alers	US 6,265,260 B1	Jul. 24, 2001
Tu	US 6,566,250 B1	May 20, 2003
Aronowitz	US 6,759,337 B1	Jul. 06, 2004
Chang (Chang '240)	US 2004/0188240 A1	Sep. 30, 2004[1]
Chang (Chang '964)	US 2005/0019964 A1	Jan. 27, 2005
Colombo	US 2005/0079696 A1	Apr. 14, 2005

ISSUES ON APPEAL

Claims 1, 6-8, 14-16, 19, and 20 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Colombo or Doyle in view of Alers or Tu, further "as evidenced" by Chang '240, Ballance, Aronowitz, or Chang '964 (Answer 3 and 4).[2]

Appellants contend that Colombo does not disclose, teach, or suggest utilizing a plasma, much less using the same plasma chamber for both the gate etch and nitridation processes (Br. 8).

Appellants contend that Doyle does not suggest that the processes of etching the gate stack and the nitridation of the etched gate stack are performed in a single plasma chamber (Br. 12).

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[1] We note that Chang '240 is mistakenly omitted in the "Evidence Relied Upon," with Chang '964 cited two times (Answer 2-3, ¶ (8)). However, we deem this error harmless since the references are correctly listed both in the Brief (page 6) and the statement of the rejection in the Answer (page 3).

[2] For purposes of judicial economy, we list the two separate rejections in the Answer as one rejection with alternate primary references, since both rejections on appeal include the same claims with the same secondary references applied for the same reasons (Br. 6; Answer 3 and 4).

Appellants further contend that the secondary references to Alers, Tu, Chang '240, Ballance, Aronowitz, and Chang '964 do not suggest application of their disclosures to plasma nitridation of gate stacks in transistors after a gate etch (Br. 8-10 and 12).

The Examiner contends that both Colombo and Doyle teach the benefits of nitridation in the presently claimed process, and that Alers and Tu show that it was conventional in the art to nitridate with a nitrogen plasma (Answer 3-6).

The Examiner contends that Chang '240, Ballance, Aronowitz, and Chang '964 are "evidence to show that 'performing both etching and nitridation in the same plasma process chamber' is ... well known in the art of semiconductor device fabrication." (Answer 6).

Accordingly, the issues presented in this appeal are as follows: (1) was it well known in this art to use a plasma containing nitrogen as a means for effecting nitridation? and (2) was it well known in this art to perform both etching and nitridation in the same plasma process chamber?

We determine that the Examiner has established a prima facie case of obviousness in view of the reference evidence. We also determine, based on the totality of the record, including due consideration of Appellants' arguments, that the preponderance of evidence weighs most heavily in favor of obviousness within the meaning of § 103(a). Therefore we AFFIRM all grounds of rejection in this appeal essentially for the reasons stated in the Answer, as well as those reasons stated below.

OPINION

We determine the following factual findings from the record in this appeal:

(1) Colombo and Doyle disclose methods for forming a field-effect transistor on a substrate, including placing a high-k dielectric layer over the substrate, a gate electrode layer over the high-k dielectric layer, and etching both layers to form a gate stack (Answer 3-4);[3]

(2) Colombo and Doyle both teach the benefits of performing a nitridation process on the gate stack, i.e., to avoid oxidation of the gate stack layers and facilitate repairing of these layers (Colombo, ¶ [0022]), or to prevent oxidation at the upper interface of the gate dielectric (Doyle, col. 5, ll. 6-9);

(3) Colombo teaches that nitridation may be accomplished by any suitable technique (¶ [0011]) and Doyle teaching nitridation by implanting nitrogen into the polysilicon gate electrode (col. 4, l. 63-col. 5, l. 6);

(4) Colombo suggests that the nitridation can be accomplished by "plasma nitridation" such as decoupled-plasma-nitridation (DPN) (page 2, claim 8, and ¶ [0011]);

(5) Colombo teaches that nitriding the sidewalls of a patterned gate structure, and forming a silicon nitride encapsulation layer along the sidewalls can be performed in sequence in a single processing chamber (¶ [0011]);

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[3] Appellants admit that this part of the claimed process is "a conventional transistor fabrication process" (Specification 1:17 – 2:2).

(6) Alers teaches that using a nitrogen containing plasma for nitridation is a conventional technique in the semiconductor art (col. 3, ll. 40-44);

(7) Tu teaches that "a conventional nitridation step is carried out by exposing the metal to a nitrogen containing plasma" (col. 6, ll. 7-11);

(8) Chang '240, Ballance, Aronowitz, and Chang '964 all teach or exemplify a single processing chamber used in sequence for two processes, e.g., etching followed by plasma deposition (Chang '240, ¶ [0040]; Ballance, col. 1, ll. 31-34; Aronowitz, col. 2, ll. 45-50, and Chang '964, ¶ [0041]).

The test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art. *See In re Young,* 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991); *In re Keller,* 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). It is well established that before a conclusion of obviousness may be made based on a combination of references, there must have been a reason, suggestion, or motivation to lead an inventor to combine these references. *See Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc.,* 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1629 (Fed. Cir. 1996).

Applying these legal principles to the factual findings on this record in this appeal, we determine that the Examiner has established a prima facie case of obviousness in view of the reference evidence. We also determine that Appellants have not adequately rebutted this prima facie case of obviousness by their arguments. As established by the factual findings listed

above, Colombo not only teaches the etching process and the benefits of the nitridation process, but further teaches using a plasma to effectuate the nitridation (factual finding (4) above). Furthermore, Colombo teaches that nitridation can be accomplished by "any suitable technique" (factual finding (3) above). Alers and Tu both teach "conventional techniques" for nitridation involving the use of a nitrogen plasma (factual findings (6) and (7) above). We determine that this teaching by Colombo would have suggested or motivated one of ordinary skill in this art to use conventional techniques such as those disclosed by Alers and Tu. We further determine that the Examiner has established that it was well known in the art to use a single processing chamber for two or more process steps. *See* factual finding (5) above, where Colombo suggests using the same process chamber for two process steps. *See* also factual finding (8) above, where the Examiner cites four references to establish that it was well known in the semiconductor fabrication art to perform etching and plasma deposition steps in the same processing chamber. We determine that the Examiner has set forth sufficient reasoning to use a single processing chamber, namely that such a step is "efficient and more cost effective" (Answer 4-6). Appellants have not disputed this reasoning (see the Brief in its entirety).

For the foregoing reasons and those stated in the Answer, we affirm both rejections on appeal. The decision of the Examiner is thus affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2006).

AFFIRMED

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